

# ASIC and FPGA Verification: A Guide to Component Modeling (Systems on Silicon)

Richard Munden



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## ASIC and FPGA Verification: A Guide to Component Modeling (Systems on Silicon)

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ASIC and FPGA Verification: A Guide to Component Modeling (Systems on Silicon) Richard Munden Richard Munden demonstrates how to create and use simulation models for verifying ASIC and FPGA designs and board-level designs that use off-the-shelf digital components. Based on the VHDL/VITAL standard, these models include timing constraints and propagation delays that are required for accurate verification of today's digital designs.

ASIC and FPGA Verification: A Guide to Component Modeling expertly illustrates how ASICs and FPGAs can be verified in the larger context of a board or a system. It is a valuable resource for any designer who simulates multi-chip digital designs.

- \*Provides numerous models and a clearly defined methodology for performing board-level simulation.
- \*Covers the details of modeling for verification of both logic and timing.
- \*First book to collect and teach techniques for using VHDL to model "off-the-shelf" or "IP" digital components for use in FPGA and board-level design verification.



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